Docket No. 100200768-1

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Remarks

This Amendment is responsive to the Office Action of **February 9, 2007**. Reexamination and reconsideration of **claims 1-18 and 20-36** is respectfully requested.

Summary of The Office Action

Claims 7-18 were allowed.

Claims 22, 26, 29, 32 and 34-36 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 1-6, 20, 21, 23, 25, 27, 28, 30, 31 and 33 were rejected under 35 U.S.C. §102(e) as being anticipated by Dodd et al. (US 6,543,883).

Claim 24 was rejected under 35 U.S.C. §103(a) as being unpatentable over Dodd et al. in view of Burke et al. (US6,102,528).

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The Present Claims Patentably Distinguish Over the References of Record

Claims 1-6, 20, 21, 23, 25, 27, 28, 30, 31 and 33 were rejected under 35 U.S.C. §102(c) as being anticipated by Dodd et al. (U.S. Patent No. 6,543,883 - assigned to the present assignee).

Independent Claim 1

The Office Action on page 3 states that the power bus element of claim 1 is taught by elements 81-83 of Dodd, but no citation from Dodd was given for the claimed feature of "being a protective layer covering the contacts of the first drive transistor." Applicant submits that elements 81-83 are not a power bus but rather define an array of transistors 85. Dodd states:

> "Each drive circuit array (81, 82, 83) includes a plurality of FET drive circuits 85 connected to respective heater resistors 56." (Dodd, column 4, lines 9-11)

Therefore array 81, 82, or 83 is not a power bus and is not a power bus electrically connected to contacts of the first drive transistor as claimed. Array 81, 82, or 83 is the drive transistors themselves and thus cannot be interpreted as a separate component (e.g. a power bus) connected to itself. Accordingly, Dodd fails to anticipate claim 1 and the rejection should be withdrawn.

Regarding the claimed feature of the power bus being "a protective layer covering the contacts of the first drive transistor," the Office Action does not cite a particular section from Dodd to support its interpretation. However since the reliance on the transistor arrays 81-83 being a power bus is incorrect, it then follows that the transistor arrays 81-83 do not teach a power bus being a protective layer. Looking to the disclosure of Dodd, it appears that power is received from conductive traces 86. This is shown in Figure 5 and is explained in column 4, lines 19-41. Applicant submits that this section fails to teach or suggest the claimed power bus.

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Accordingly, Dodd fails to anticipate claim 1 for this additional reason and the rejection should be withdrawn.

Regarding the claimed first and second heater elements, the associated first and second drive transistors, and the recited spacing configurations, the Office Action (on page 3) cites to Dodd Figure 8 and heater resistors 56 and FET drive circuits 85. Applicant notes that Figure 6A of Dodd shows a more detailed view of single heater resistor 56 and FET drive circuit 85 combination.

Looking to the spacings disclosed by Dodd, Figure 8 (or the other figures) does not show different spacings as claimed. Figure 8 appears to illustrate the resistors 56 and drive circuits 85 (not labeled) to be evenly spaced, not differently. Of course, patent figures are not determinative for features such as relative sizes, dimensions, and spacings so one must look to the specification for clarification of the actual teachings.

In the specification, Dodd does not elaborate on the spacing between the heater resistors 56 and transistor arrays 81, 82, 83, or the FET drive circuits 85. Dodd does discuss spacing between the groups of drop generators 61, 62, 63 and resistors 56 (column 3, lines 36-56) and the spacing of the feed slots 71, 72, 73 (column 3, lines 63-67). However, Applicant does not find a disclosure that teaches the claimed arrangement of heater elements and drive transistors.

Therefore, Dodd fails to teach each and every element of claim 1 and fails to support a prima facie §102 rejection. The rejection should be withdrawn and claim 1 allowed. Accordingly, dependent claims 2-6 also patentably distinguish over the reference and are in condition for allowance.

Dependent Claim 6

Claim 6 depends from claim 1 and recites that the first distance is a heater element centerline-to-centerline spacing, and the second distance is a transistor center-to-centerline spacing. The Office Action cites Dodd Figures 6A, 6B, and 8 as teaching these features. However, Figure 6A illustrates a single combination of one heater resistor 56 and one FET drive

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circuit 85. Since two or more resistors 56 are not shown, a resister centerline-to-centerline spacing is not disclosed. Likewise since two or more transistors 85 are not shown, a transistor center-to-centerline spacing is not disclosed. Similarly, Figure 6B illustrates only a single combination of one heater resistor 56 and one FET drive circuit 85, and thus centerline-to-centerline spacings are not disclosed. Figure 8 does illustrate multiple heater resistors 56 and multiple FET drive circuits 85 (not labeled) but at best it appears that the elements are evenly spaced with regard to their centerlines. Furthermore, nothing in the corresponding text of the disclosure teaches the claimed arrangement in order to support an anticipation rejection. Dodd column 3, lines 37-41 refers to a predetermined center to center spacing for the heater resistors 56 but does not discuss an arrangement or relationship to the drive circuits 85 as claimed. Thus, claim 6 is not anticipated by Dodd and the rejection should be withdrawn.

Independent Claim 20

The Office Action on page 4 cites Figures 6A and 6B as teaching the claimed fluid ejection device. Figure 6A is an embodiment of Figure 6 where the width of the transistor 85 is extended in a direction towards the resistor 56 (column 4, lines 44-46). Figure 6B is another embodiment of Figure 6 where the transistor 85 is shifted in a direction towards the resistor 56 (column 5, lines 21-23).

As explained above, Figure 6A illustrates a single combination of one heater resistor 56 and one FET drive circuit 85. A vertical column of resisters 56 is not shown and a vertical column of associated transistors 85 is not shown. Thus, a centerline-to-centerline comparison between two groups of elements in vertical columns is not illustrated and cannot be made. Therefore, Figure 6A fails to teach claim 20.

Similarly, Figure 6B illustrates a single combination of one heater resistor 56 and one FET drive circuit 85. A vertical column of resisters 56 is not shown and a vertical column of associated transistors 85 is not shown. Thus, a centerline-to-centerline comparison between two groups of elements in vertical columns is not illustrated and cannot be made. Therefore, Figure 6B fails to teach claim 20.

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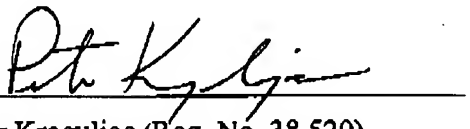
Accordingly, Dodd fails to teach each and every element of claim 20 and fails to establish a prima facie anticipation rejection. The rejection should be withdrawn and claim 20 should now be allowed. As such, a prima facie rejection of dependent claims 21, 23, 24, 27, 28, 30, 31 and 33 based on Dodd has not been established and the rejection of these claims should be withdrawn.

Conclusion

For the reasons set forth above, **claims 1-18** and **20-36** patentably and unobviously distinguish over the references of record and are now in condition for allowance. An early allowance of all claims is earnestly solicited.

Respectfully submitted,



Peter Kraguljac (Reg. No. 38,520)
(216) 348-5843
McDonald Hopkins LLC
600 Superior Avenue, E.
Suite 2100
Cleveland, OH 44114

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